PATENT

UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Applicant: ANDERSON et al.

Application: **METHOD, APPARATUS, AND COMPUTER PROGRAM PRODUCT FOR IMPLEMENTING DETERMINISTIC BASED BROKEN SCAN CHAIN DIAGNOSTICS**

Serial No.: 10/821,160

Filing Date: April 8, 2004

Art Unit: 2138

Examiner: Saqib Javaid Siddiqui

Case: ROC920030422US1

APPEAL BRIEF FOR APPLICANTS

JOAN PENNINGTON
535 North Michigan Avenue
Unit 1804
Chicago, Illinois 60611

One of the Attorneys for Applicants

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535 North Michigan Avenue
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APPEAL BRIEF FOR APPLICANTS

Sir:

This is an appeal of the final rejections of all the claims 1-2, 4-13, and 15-20 in the office action made final and mailed July 27, 2007. For the reasons set forth below, it is submitted that the Board should reverse the final rejections of claims 1-2, 4-13, and 15-20.

(1) REAL PARTY IN INTEREST

The real party of interest is International Business Machines Corporation.

(2) RELATED APPEALS AND INTERFERENCES

Applicants' attorney knows of no other appeals or interferences that would have a bearing on the Board's decision in the present appeal.

(3) STATUS OF CLAIMS

Claims 1-2, 4-13, and 15-20 have been finally rejected under 35 U.S.C. § 103(a) in an office action mailed July 27, 2007. The rejection of each of the claims 1-2, 4-13, and 15-20 has been appealed.

(4) STATUS OF AMENDMENTS

No amendment was filed after the final rejection.

(5) SUMMARY OF CLAIMED SUBJECT MATTER

The claimed invention as recited by independent claims 1, 13 and 19, and representative separately patentable dependant claims 9, 10, and 11, can best be appreciated and understood with reference to the patent specification (hereinafter page p., line l.).

The present invention solves a continuing problem for VLSI testing of how to diagnose an exact location of broken scan chain or chains. When there is low or zero yield, the scan chains are often broken so that the only opportunity to learn and diagnose the root cause of the problem is defect localization based upon scan chain failure data. Other known test applications, such as, Level Sensitive Scan Design (LSSD), Logic Built In Self Test (LBIST), Array Built In Self Test (ABIST), functional,

Design-For-Test (DFT) and Design-For-Diagnostics (DFD), all assume the scan chains are operational. The problem of a broken scan chain or chains is usually encountered early in a technology life cycle and diagnostics is critical in improving the fabrication process so that manufacturing yield levels can be quickly achieved. An inability to improve the technology and yield can greatly impact a program or at least severely minimize the revenue that could be realized. (p. 1, l. 10-23)

Significant drawbacks are that the known solutions require very large data volumes, extremely long simulation times, and are not always 100% reliable, and further not one single known method is always successful all the time. This can be attributed to the nature of the particular fault and its manifestation, complex faults, and that faults are not limited to the type of chip area that propagates to system paths of the broken latch or latches whether it originates from combinational logic or array outputs. (p. 1, 2. 21-27)

The present invention provides an admittedly novel method, apparatus and computer program product for implementing deterministic based broken scan chain diagnostics. (p. 3, l. 6-23)

Independent claim 1 recites a method for implementing deterministic based broken scan chain diagnostics using a computer test system connected to a Physical Failure Analysis system comprising the steps of: (p. 3, l. 6-23)

generating a deterministic test pattern using a base deterministic test pattern set generated by an Automatic Test Pattern Generation (ATPG) system; the deterministic test pattern being a predetermined Level Sensitive Scan Design (LSSD) pattern; (p. 3, l.

6-23; p. 7, l. 4-34; p. 8, l. 1-5)

utilizing all potential system functional paths and all system clocks on a device under test, loading the deterministic test pattern into each scan chain in the device under test in a system mode using lateral insertion of respective deterministic values of the deterministic test pattern into each of a plurality of latches of each said scan chain via system data ports and applying system clocks to capture the respective deterministic values in each of the plurality of latches of each said scan chain; (p. 3, l. 6-23; p. 5, l. 30-34; p. 6, l. 1-9, 23-34; p. 7, l. 5-25)

unloading each scan chain and identifying a last switching latch in each said scan chain; (p. 3, l. 6-23; p. 8, l. 7-8)

repeating the generating, loading, unloading and identifying a last switching latch in each said scan chain testing steps a selected number of times with the deterministic test pattern; (p. 3, l. 6-23; p. 7, l. 4-31)

checking for consistent results of the identified last switching latch in each scan chain; and responsive to consistent results being identified, sending the identified last switching latch in each scan chain to said Physical Failure Analysis system to localize a physical defect; and (p. 3, l. 6-23; p. 7, l. 4-31; p. 9, l. 22-32)

responsive to consistent results not being identified, selecting another deterministic test pattern. (p. 3, l. 6-23; p. 9, l. 22-32)

In accordance with features of the invention, the deterministic test function is used in a lateral broadside insertion manner across all latch system data ports and efficiently analyze the response data such that switching and non-switching latches are

readily identified with the next to last non-switching latch being the point of the break within the defective scan chains. This comprehensive latch perturbation in conjunction with interactive diagnostic algorithms is used to identify and pinpoint the defective location in the broken scan chain. The LSSD scan A, B clocks and system C1, C2 clocks are assumed to be functional. This deterministic test function and ultimately deterministic test patterns derived thereof, can take on different forms and origins, some external to product and some internal to product. Four embodiments of the basic concept are provided depending upon the level of test generation support from the specific design structure. (p. 6, l. 22-34)

Dependent claim 9 recites a method for implementing deterministic based broken scan chain diagnostics as recited in claim 1 wherein the step of loading the deterministic test pattern into each scan chain in the device under test using lateral insertion via system data ports and applying system clocks includes the steps of applying deterministic values of the deterministic test pattern to a selected one of scan chain inputs and primary inputs of latches within each scan chain. (p. 3, l. 6-23; p. 6, l. 22-34)

Dependent claim 10 recites a method for implementing deterministic based broken scan chain diagnostics as recited in claim 1 wherein the step of loading the deterministic test pattern into each scan chain in the device under test using lateral insertion via system data ports and applying system clocks includes the steps of applying perturbation deterministic values of the deterministic test pattern to a selected

one of scan chain inputs and primary inputs of latches within each scan chain. (p. 3, l. 6-23; p. 6, l. 22-34. p. 8, l. 8-19)

Dependent claim 11 recites a method for implementing deterministic based broken scan chain diagnostics as recited in claim 1 wherein the step of loading the deterministic test pattern into each scan chain in the device under test using lateral insertion via system data ports and applying system clocks includes the steps of applying random data from a software Pseudo Random Pattern Generator (PRPG) to scan chain inputs and primary inputs of latches within each scan chain. (p. 3, l. 6-23; p. 6, l. 22-34; p. 8, l. 31 -p. 9, l. 6)

Independent claim 13 recites apparatus for implementing deterministic based broken scan chain diagnostics in a computer test system connected to a Physical Failure Analysis system comprising: (p. 3, l. 6-23)

a set of deterministic test patterns; said set of deterministic test patterns being generated using a base deterministic test pattern set generated by an Automatic Test Pattern Generation (ATPG) system in a computer test system; each of the deterministic test pattern being a predetermined Level Sensitive Scan Design (LSSD) pattern; (p. 3, l. 6-23; p. 5, l. 30-34; p. 6, l. 1-9, 23-34; p. 7, l. 5-25)

a test control program utilizing all potential system functional paths and all system clocks on a device under test, loading a deterministic test pattern into each scan chain in the device under test in a system mode using lateral insertion of respective deterministic values of the deterministic test pattern into each of a plurality of latches of each said scan chain via system data ports and applying system clocks to capture the

respective deterministic values in each of the plurality of latches of each said scan chain; unloading each scan chain and identifying a last switching latch in each scan chain; repeating the generating, loading, unloading and identifying a last switching latch in each said scan chain testing steps a selected number of times with the deterministic test pattern; and checking for consistent results of the identified last switching latch in each scan chain and responsive to consistent results being identified, sending the identified last switching latch in each scan chain to said Physical Failure Analysis system to localize a physical defect; and responsive to consistent results not being identified, selecting another deterministic test pattern. (p. 5, l. 1-14; p. 5, l. 30-34; p. 6, l. 1-9, 23-34; p. 7, l. 5-25; p. 9, l. 22-32)

Independent claim 19 recites a computer program product for implementing deterministic based broken scan chain diagnostics of a device under test in a computer test system connected to a Physical Failure Analysis system, said computer program product including instructions stored on a computer recording medium consisting one of a floppy disk, an optically read compact disk, a compact disk read only memory (CD-ROM), and a tape, wherein said instructions, when executed by the computer test system to cause the computer system to perform the steps of: (p. 3, l. 6-23)

generating a deterministic test pattern using a base deterministic test pattern set generated by an Automatic Test Pattern Generation (ATPG) system; the deterministic test pattern being a predetermined Level Sensitive Scan Design (LSSD) pattern; (p. 3, l. 6-23; p. 7, l. 4-34; p. 8, l. 1-5)

utilizing all potential system functional paths and all system clocks on a device under test, loading the deterministic test pattern into each scan chain in the device under test in a system mode using lateral insertion of respective deterministic values of the deterministic test pattern into each of a plurality of latches of each said scan chain via system data ports and applying system clocks to capture the respective deterministic values in each of the plurality of latches of each said scan chain; (p. 3, l. 6-23; p. 5, l. 30-34; p. 6, l. 1-9, 23-34; p. 7, l. 5-25)

unloading each scan chain and identifying a last switching latch in each scan chain; (p. 3, l. 6-23; p. 8, l. 7-8)

repeating the generating, loading, unloading and identifying a last switching latch in each said scan chain testing steps a selected number of times with the deterministic test pattern; (p. 3, l. 6-23; p. 7, l. 4-31)

checking for consistent results of the identified last switching latch in each scan chain; and responsive to consistent results being identified, sending the identified last switching latch in each scan chain to said Physical Failure Analysis system to localize a physical defect; and (p. 3, l. 6-23; p. 7, l. 4-31; p. 9, l. 22-32)

responsive to consistent results not being identified, selecting another deterministic test pattern. (p. 3, l. 6-23; p. 9, l. 22-32)

In accordance with features of the invention, a deterministic pattern set and functions are used to generate broken scan chain diagnostic patterns. For example, upon loading the scan chains it is clear to see that a stuck-at-1 fault causes the remainder of the associated scan chains to be also stuck-at-1. Upon pulsing the

system clocks C1 CLK and C2 CLK, system data is clocked in broadside via the system data ports of the latches within the scan chains of the device under test 128. Subsequently, the scan chains are then unloaded and the scan chain internal states are analyzed by tester resident software that identifies the latch at which the deterministic data stops and the stuck-at-0 or stuck-at-1 data begin. This unload data can also be compared against known correct reference unload data, if available. Comparing expected results from a good reference device with the bad device helps narrow down or localize where the fault occurs and thus, greatly improves the accuracy of the diagnostic call. In addition, executing a large number of deterministic test patterns, for example, 100 tester loops across unique clocking sequences or base pattern sets also provides improved diagnostic granularity. The exact number of deterministic patterns to be applied can also be arrived at empirically on a design-by-design basis. The more deterministic test patterns applied resulting in the last switching latch to be reported as common mode provides even greater confidence of the diagnostic call. In some embodiments, deterministic test patterns are generated on-the-fly to easily and efficiently sensitize, capture, and ultimately observe the defect. (p. 4, l. 4-26)

FIG. 3 illustrates a typical LSSD scan chain 300 including a chain of Shift Register Latches (SRLs), SRL1-SRLN, each including a master latch L1, 302 and a slave latch L2, 304. The master latch L1, 302 has a pair of data ports SCAN and DATA, that may be captured by the latch responsive either to a first scan clock A CLK or a first functional system clock C1 CLK. The slave latch L2, 304 captures the value stored in the master latch L1, 302 responsive to either a second scan clock B CLK or a second

functional system clock C2 CLK. As shown in FIG. 3, the second scan clock B CLK and the second functional system clock C2 CLK are combined as a single clock signal B/C2 CLK. The second scan clock B CLK and the second functional system clock C2 CLK are typically driven out of phase with both the first scan clock A CLK and the first functional system clock C1 CLK applied to the master latch L1, 302. (p. 5, l. 30-p. 6, l. 9)

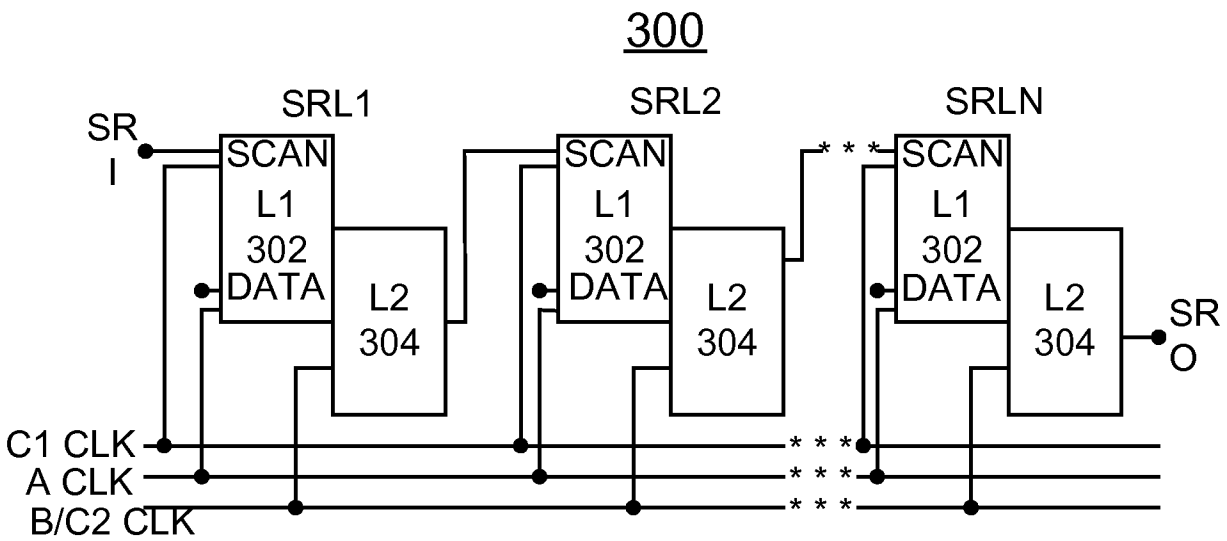

FIG. 3

FIG. 4, there are shown exemplary steps for implementing deterministic based broken scan chain diagnostics in accordance with the preferred embodiment starting at a block 400 and repeated a selected number N of times as indicated at a block 402. A deterministic test pattern is generated as indicated at a block 404. As

indicated at a block 406, a first embodiment utilizes an existing base deterministic test pattern set (LSSD Test Mode) that is generated by an available ATPG system. (p. 7, l. 27-34)

As indicated at a block 408, a second embodiment uses perturbations of a single base deterministic test pattern from the same ATPG system. . FIG. 5 illustrates a base set of deterministic pattern vectors 502 in conjunction with a perturbation matrix 504 that are applied to an exclusive OR (XOR) 506 to automatically generate diagnostic broken scan chain patterns applied to scan chains as indicated at a block 508. Referring also to FIG. 6, there is shown a sample of a set of deterministic test patterns generally designated by the reference character 600 generated in this manner with the no invert, all invert, and nth bit functions. As indicated at a block 410, a third embodiment utilizing a software Pseudo Random Pattern Generator (PRPG) to generate these deterministic test patterns 134. A fourth embodiment, which is probably the most powerful, fully incorporates the perturbation function in conjunction with a small set of base deterministic patterns 134 to be resident on-chip. (p.8, l. 8 - p. 9. l. 9)

In all cases, the concept is to apply deterministic test patterns in a system mode, where the data values are laterally inserted into the latches of the scan chains utilizing all potential system functional paths and all system clocks on the product. Minimal, if any, test generation is required. (p. 9, l. 22)

The generated deterministic test pattern is loaded into the scan chains as indicated at a block 412 and then system clocks C1 CLK and C2 CLK are applied as indicated at a block 414. The scan chains are unloaded as indicated at a block 316. A

last switching latch is identified as indicated at a block 418. After these steps are repeated N times as indicated at a decision block 420, then checking for consistent results is performed as indicated at a decision block 422. If the results are consistent, then the identified last switching latch is sent to a Physical Failure Analysis (PFA) to localize the physical defect as indicated at a block 424. When the results are not consistent, then another deterministic test pattern is applied as indicated at a block 426. Then the exemplary steps are repeated. (p. 9, l. 22-32).

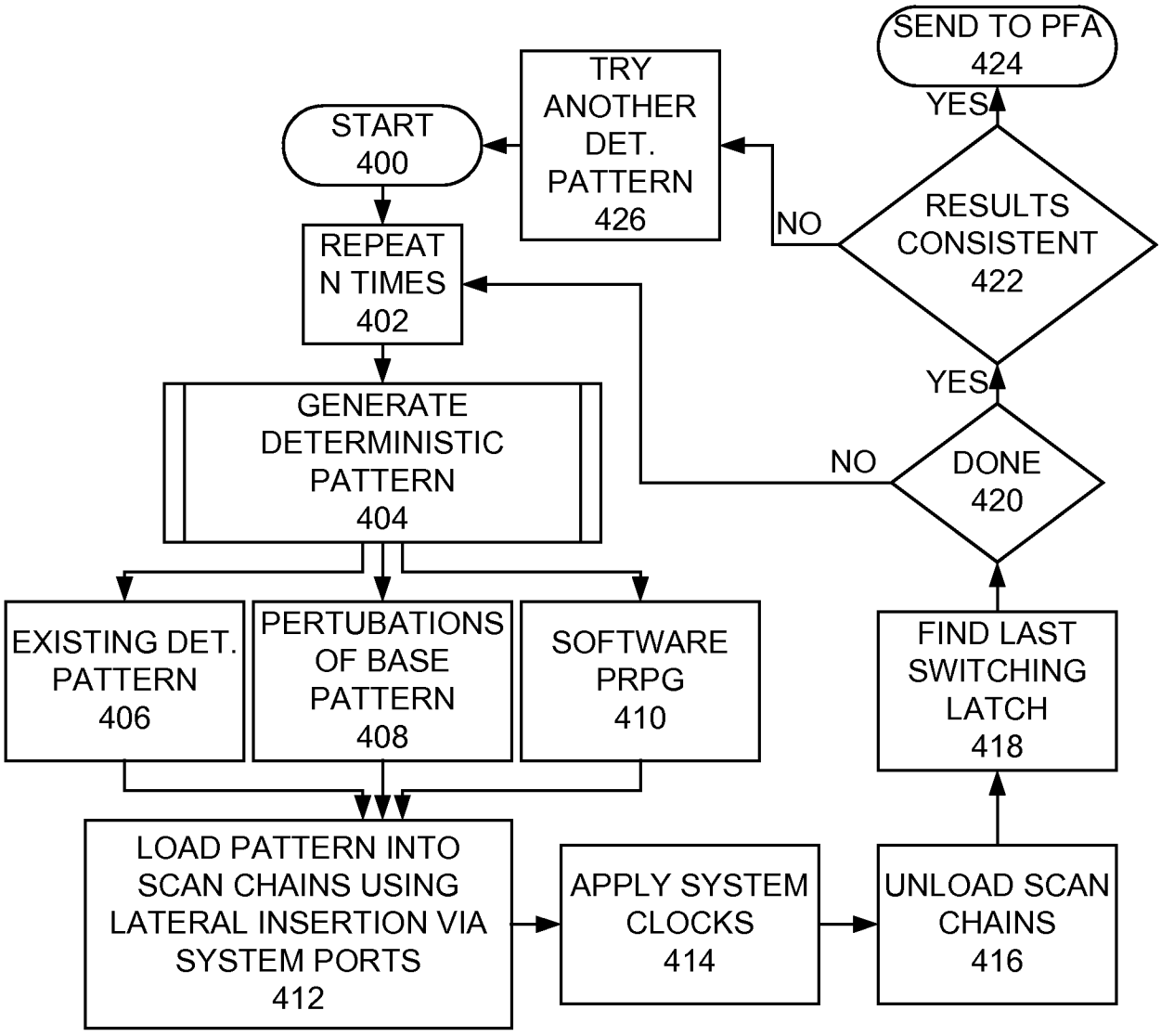

FIG. 4

In brief, the method of the invention is very valuable in diagnosing broken scan chains, especially for VLSI designs not containing BIST structures which prior art methods and techniques rely upon to solve this problem. These BIST-based methods are also not always 100% successful due to the nature of the defect or rather simply,

not sufficient to expose/sensitize the actual defect mechanism causing the broken scan chain. In addition, this concept is very powerful in certain situations where either the BIST structures themselves are defective and/or do not propagate to certain sections of combinational logic, or arrays/memory that feed the latches of interest within the broken scan chain(s). The method of the invention is primarily independent of design type, with no LBIST, ABIST, DFT, and DFD structures required, other than being LSSD compliant. (p. 9, l. 33 - p. 10, l. 11)

The method of the invention is superior to other methods because it provides an efficient and unique solution to the stuck-at or broken scan chain diagnostics within a Deterministic environment with the following benefits. Rapid on-the-fly diagnosis is provided and defective latch is located with high probability. The method of the invention is compatible with existing non-BIST designs (ASICs) and is compatible with existing structural LSSD, and BIST designs. The method of the invention eliminates extensive test result data collection and implementation is relatively simple. The method of the invention is easily simplified and automated for manufacturing test. The method of the invention provides a quick and direct path from the computer test system 100 to Physical Failure Analysis. The method of the invention can be an on-chip hardware implementation for use as a BIST support function and DFD features. Fault simulation is not required with the method of the invention. (p. 10, l. 12-25)

Furthermore, the method of the invention is highly effective when diagnosing un-modeled faults, AC defects, and intermittent fails that do not conform to

the classical or conventional stuck-at or transitional fault models. Also, many of the underlying basic concepts can be generalized and integrated into general-purpose automated test generation and diagnostic products. (p. 10, l. 26-31)

(6) GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The single ground of rejection presented for review is the rejection of claims 1-2, 4-13, and 15-20 under 35 USC §103(a) as being unpatentable over Sarrica et al. publication entitled, "Theory and Implementation of LSSD scan ring & STUMPS channel Test and Diagnosis" in view of Rajski, U.S. patent 6,662,327.

(7) ARGUMENT

A. INTRODUCTION

Applicants respectfully submit that the Examiner's rejections of all pending claims 1-2, 4-13, and 15-20 under 35 U.S.C. § 103(a) should be reversed because the subject matter of each of the independent claims 1,13, and 19 and the representative dependant claims 9, 10, and 11 is patentable over all the references of record. There is no teaching or suggestion in any of the cited references, individually or taken as a whole, to make the claimed invention obvious. The rejections of all of the pending claims 1-2, 4-13, and 15-20 under 35 U.S.C. §103(a) are improper and should be reversed.

B. THE SCOPE AND CONTENT OF THE PRIOR ART

The cited Sarrica et al. publication discloses a level sensitive scan design (LSSD) including L1 L2 shift register latches (SRLs) test process. A LSSD scan ring with for

SRLs is illustrated for tests which require a test control module (TCM) to operate in the LSSD scan mode. STUMPS (Self-Test Using a MISR and a Parallel Shift register sequence generator) channels are connected to the SRLs in a Self-Test Scan mode. A pseudo-random pattern generator (PRPG) and a multiple input signature register (MISR) are connected to the scan channels. In an Array scan mode, certain latches on the TCM are designated as address stepper SRLs, while these SRLs are removed from the chains when array initialization is performed. The address stepper SRLs supply the addresses for the arrays. Self-test scan tests performed with the SRLs configured into STUMPS channels include ABT1 and ABT2. Lateral insertion is illustrated in Figure 6, and is used for finding a SRL with a stuck at fault. Lateral insertion analysis is described as being repeated with scan diagnostics running 255 pseudo-random patterns in self-test scan STUMP mode to find the location of a stuck-at-fault.

Rajski, U.S. patent 6,662,327 discloses a method for clustered pattern generation that maintains high fault coverage of a circuit under test while it reduces the amount of test data to store by using clusters of correlated test patterns. A test pattern generator stores only a small number of center test vectors which serve as centers of clusters. The generator applies each center test vector to a circuit under test multiple times. However, every time the center vector is shifted into the circuit, some of its positions are complemented. The cluster may have a number of spheres which correspond to test vectors derived with various diffraction probabilities and computed to maximize fault coverage, minimize the total number of clusters, and reduce the test application time. The method also encodes several partially specified center test

vectors in scan path using the polarity between scan cells, scan order and waveform generators controlling scan inputs. Stated at column 5, lines 45-66:

> FIG. 1 is a flowchart of a method for testing such a circuit according to the invention. A computer program or equivalent device reads the ideal description of a circuit to be tested (30) and computes clusters of test patterns (32). Each cluster consists of a center pattern and a number of other patterns derived from the center pattern by complementing some of its positions. From the test patterns and the ideal circuit description, expected circuit signatures are computed for later comparison against actual signature (34).
>
> A tester then tests an actual circuit by applying the clusters of test patterns. The tester, however, does not have to store the clusters. Instead, it stores only the center test patterns, the diffraction probabilities, and an initial seed. In addition, a seed and a polynomial are stored so that a diffractor circuit can reproduce exactly the same sequence of patterns as the ones produced for the ideal circuit. The tester applies the center patterns repeatedly, every time complementing some positions in a pseudorandom manner (36). The process is fully deterministic, i.e. the tester reproduces exactly the same patterns as the ones computed as part of the test of the ideal circuit. The tester also computes the actual signature from the responses of the device under test (38). The actual signature is then compared to the circuit's expected signature (40). If the signatures match, the circuit is declared good; if they do not, the circuit is considered faulty.

C. THE REJECTION OF CLAIMS 1-2, 4-13, and 15-20 UNDER 35 USC 103 SHOULD BE REVERSED

The Board should reverse the rejection of the claims 1-2, 4-13, and 15-20 under 35 USC §103 over the Sarrica et al. publication in view of Rajski, U.S. patent 6,662,327.

Claim 1 is patentable

35 U.S.C. §103 requires that the invention as claimed be considered "as a whole" when considering whether the invention would have been obvious when it was made. Graham v. John Deere, 383 U.S. 1, 148 USPQ 459, 472 (1966). It is applicants'

claimed invention which must be considered as a whole pursuant to 35 U.S.C. §103, and failure to consider the claimed invention as a whole is an error of law. The legal determination under section 103 is whether the claimed invention as a whole would have been obvious to a person of ordinary skill in the art at the time the invention was made.

Independent claim 1 recites a method for implementing deterministic based broken scan chain diagnostics using a computer test system connected to a Physical Failure Analysis system. Independent claim 1 recites that the deterministic test pattern being a predetermined Level Sensitive Scan Design (LSSD) pattern; and utilizing all potential system functional paths and all system clocks on a device under test, loading the deterministic test pattern into each scan chain in the device under test in a system mode using lateral insertion of respective deterministic values of the deterministic test pattern into each of a plurality of latches of each said scan chain via system data ports and applying system clocks to capture the respective deterministic values in each of the plurality of latches of each said scan chain.

Only applicants teach the subject matter of the invention, as recited by pending independent claim 1. The invention as claimed must be considered "as a whole" when considering whether the invention would have been obvious when it was made. The prior art references of record provide no teaching, suggestion or inference in the prior art as a whole or knowledge generally available to one having ordinary skill in the art to achieve the claimed invention.

Applicants only teach these steps.

Sarrica teaches applying only scan clocks with lateral insertion analysis, not utilizing all system clocks, as is taught and claimed by Applicants with lateral insertion analysis. Applicants respectfully submit that both the cited Sarrica publication and Rajski patent utilize the scan chain to perform device tests. Applicants respectfully submit that the cited Sarrica publication and Rajski patent do not enable, nor suggest utilizing all potential system functional paths and all system clocks on a device under test, loading the deterministic test pattern into each scan chain in the device under test in a system mode using lateral insertion of respective deterministic values of the deterministic test pattern into each of a plurality of latches of each said scan chain via system data ports and applying system clocks to capture the respective deterministic values in each of the plurality of latches of each said scan chain, as recited in the independent claim 1.

Applicants respectfully that independent claim 1 is patentable over all the references of record. The total teachings of the cited references fail to render obvious the subject matter of the present invention as defined in independent claim 1.

The present invention provides a solution which speeds broken scan chain diagnostics on the majority of the failing devices to enable timely process corrections and yield improvements.

Applicants teach and claim recites unloading each scan chain and identifying a last switching latch in each scan chain; repeating the generating, loading, unloading and identifying a last switching latch in each said scan chain testing steps a selected number of times with the deterministic test pattern; and checking for consistent results

of the identified last switching latch in each scan chain. The references of record including Sarrica et al. and Rajski fail to suggest generating, loading, and unloading testing steps a selected number of times with the deterministic test pattern; and checking for consistent results. Further the steps of checking for consistent results of the identified last switching latch in each scan chain; and responsive to consistent results being identified with the deterministic test pattern, sending the identified last switching latch in each scan chain to the Physical Failure Analysis system to localize the physical defect are only taught by Applicants.

These limitations as recited in independent claim 1 are not disclosed or suggested by the combined teachings of Sarrica et al. and Rajski. Neither Sarrica et al. nor Rajski disclose checking for consistent results of the identified last switching latch in each scan chain. Neither Sarrica et al. nor Rajski provide any equivalent testing steps.

In order for there to be a prima facie showing of obviousness under 35 U.S.C. §103, it is necessary that the references being combined in an attempt to demonstrate prima facie obviousness must themselves suggest the proposed combination. For a combination of prior art references to render an invention obvious, "[t]here must be some reason, suggestion, or motivation found in the prior art whereby a person of ordinary skill in the field of the invention would make the combination." In re Oetiker, 977 F.2d 1443, 1447, 24 USPQ2D 1443, 1446 (Fed. Cir. 1992). It is insufficient to establish obviousness that the separate elements of the invention existed in the prior art, absent some teaching or suggestion, in the prior art, to combine the elements.

Arkie Lures, Inc. v. Gene Larew Tackle, Inc., 119 F.3d 953, 957, 43 USPQ2d 1294, 1297 (Fed. Cir. 1997).

The motivation, suggestion or teaching may come explicitly from statements in the prior art, the knowledge of one of ordinary skill in the art, or, in some cases the nature of the problem to be solved. In re Kotzab, 217 F.3d 1365, 1370, 55 USPQ2d 1313, 1317 (Fed. Cir. 2000). Hindsight in impermissible when an examiner rejects an application in reliance upon teachings not drawn from any prior art disclosure, but from the applicant's own disclosure. In re Dembiczak, 175 F.3d 994, 998, 50 USPQ2d 1614, 1616 (Fed. Cir. 1999). Broad conclusory statements standing alone are not "evidence." Id.

The test for obviousness is what the combined teachings of the references would have suggested to one of ordinary skill in the art. See In re Young, 927 F.2d 588, 591, 18 USPQ2d 1089, 1091 (Fed. Cir. 1991).

The ultimate determination of whether an invention would have been obvious under 35 USC § 103(a) is a legal conclusion based on underlying findings of fact. In re Kotzab, 217 F.3d 1365, 1370, 55 USPQ2d 1313, 1317 (Fed. Cir. 2000). The claimed invention is unpatentable if the differences between it and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art.

In a proper obviousness determination, "whether the changes from the prior art are 'minor', . . . the changes must be evaluated in terms of the whole invention, including whether the prior art provides any teaching or suggestion to one of ordinary

skill in the art to make the changes that would produce the patentee's . . . device." This includes what could be characterized as simple changes, as in In re Gordon and Sutherland, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1983) (Although a prior art device could have been turned upside down, that did not make the modification obvious unless the prior art fairly suggested the desirability of turning the device upside down.).

The total teachings of Sarrica and Rajski provide no motivation, suggestion or teaching to support the Examiner's proposed modifications to provide the claimed invention, as taught by Applicants. Applicants respectfully submit that the subject matter of independent claim 1 is novel and is not rendered obvious by the references of record.

The total teachings of the references of record including Sarrica and Rajski, considered together in combination, do not provide any remote suggestion of the recited subject matter of independent claim 1.

A prior art reference may be considered to teach away when "a person of ordinary skill, upon reading the reference, would be discouraged from following the path set out in the reference, or would be led in a direction divergent from the path that was taken by the applicant." In re Gurley, 27 F.3d 551, 553, 31 USPQ2D 1130, 1131 (Fed. Cir. 1994). The above-recited limitations of independent claim 1 also are not shown nor suggested in total combination of Sarrica and Rajski.

Thus, independent claim 1 is patentable.

Hindsight is impermissible when an examiner rejects an application in reliance upon teachings not drawn from any prior art disclosure, but from the applicant's own

disclosure. In re Demiski, 796 F.2d 236,443, 230 USPQ2d 313, 316 (Fed. Cir. 1986); W.L. Gore & Assocs. Inc. V. Garlock, Inc., 721 F.2d 1540, 1553, 220 USP1 303, 313 (Fed. Cir. 1984), cert. denied, 469 U.S. 851 (1984).

That one must point to some reason, suggestion, or motivation to make a combination is not to say that the teaching must be explicit, but in order to render an invention obvious by the combination of prior art references, the prior art must contain some reason, suggestion, or motivation. It is impermissible to use the inventor's disclosure as a "road map" for selecting and combining prior art disclosures. In Interconnect Planning Corp. v. Feil 774 F.2d 1132, 1143, 227 USPQ 542, 551 (Fed. Cir. 1985), the Federal Circuit noted, "The invention must be viewed not with the blueprint drawn by the inventor, but in the state of the art that existed at the time."

The prior art of record provides no teaching, suggestion or inference in the prior art as a whole or knowledge generally available to one having ordinary skill in the art to achieve the claimed invention, when the invention as claimed is considered "as a whole" as required by 35 U.S.C. § 103 when considering whether the invention would have been obvious when it was made. Graham v. John Deere, 383 U.S. 1, 148 USPQ 459, 472 (1966).

In the words of the Court of Appeals for the Federal Circuit, "The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification." In re John R. Fritch, 972 F.2d 1260, 1266, 23 USPQ2d 1780 (Fed. Cir. 1992). See In re Gordon and Sutherland, 733 F.2d 900, 221 USPQ 1125, 1127 (Fed.

Cir. 1984), Carl Schenck, A.G. v. Nortron Corp., 713 F.2d 782, 787, 218 USPQ 698, 702 (Fed. Cir. 1983), and In re Sernaker, 702 F.2d 989, 995-96, 217 USPQ 1, 6-7 (Fed. Cir. 1983).

Applicant respectfully submits that the prior art descriptions of Sarrica and Rajski falls short of applicant's invention, and the subject matter of the claimed invention as recited in claim 1 would not have been obvious to one of ordinary skill in the art.

Thus, independent claim 1 is patentable.

Claim 9 is patentable

Dependent claim 9 is patentable for the same reasons as claim 1. Dependent claim 9 recites that the step of loading the deterministic test pattern into each scan chain in the device under test using lateral insertion via system data ports and applying system clocks includes the steps of applying deterministic values of the deterministic test pattern to a selected one of scan chain inputs and primary inputs of latches within each scan chain.

The references of record do not suggest the subject matter of the invention as recited by claim 9. In Re Fritch 972 F.2d at 1266, 23 USPQ2d at 1780 (Fed. Cir. 1992), states: "[I]t is impermissible to use the claimed invention as an instruction manual or 'template' to piece together the teachings of the prior art so that the claimed invention is rendered obvious. ... This court has previously stated that '[o]ne cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention." Applicants respectfully submit that the total teaching of Sarrica and Rajski would not achieve the claimed invention as recited by claim 9.

Sarrica and Rajski considering the total teachings, fail to suggest applying deterministic values of the deterministic test pattern to a selected one of scan chain inputs and primary inputs of latches within each scan chain as required by dependent claim 9.

Applicant respectfully submits that no teaching or motivation exists for one of ordinary skill in the art to modify the prior art description of Sarrica and Rajski to achieve the subject matter of the claimed invention as recited in claim 9. Only with the use of applicant's own disclosure, rather than relying upon teachings drawn from any prior art disclosure, would the prior art be modified in the manner suggested by the Examiner. The claimed invention is not rendered obvious by the mere fact that the prior art could be modified in the manner suggested by the Examiner. The prior art fails to suggest the desirability of the modification. No teaching, suggestion, or motivation is provided by Sarrica and Rajski and no general knowledge in the art exists to achieve the subject matter of the invention, as claimed by Applicants in dependent claim 9.

Thus, dependent claim 9 is patentable.

Claim 10 is patentable

Dependent claim 10 is patentable for the same reasons as claim 1. Dependent claim 10 recites that the step of loading the deterministic test pattern into each scan chain in the device under test using lateral insertion via system data ports and applying system clocks includes the steps of applying perturbation deterministic values of the deterministic test pattern to a selected one of scan chain inputs and primary inputs of latches within each scan chain.

The references of record do not suggest the subject matter of the invention as recited by claim 10.

Sarrica and Rajski considering the total teachings, fail to suggest perturbation deterministic values of the deterministic test pattern to a selected one of scan chain inputs and primary inputs of latches within each scan chain as required by dependent claim 10.

Thus, dependent claim 10 is patentable.

Claim 11 is patentable

Dependent claim 11 is patentable for the same reasons as claim 1. Dependent claim 11 recites that the step of loading the deterministic test pattern into each scan chain in the device under test using lateral insertion via system data ports and applying system clocks includes the steps of applying random data from a software Pseudo Random Pattern Generator (PRPG) to scan chain inputs and primary inputs of latches within each scan chain.

The references of record do not suggest the subject matter of the invention as recited by claim 11. It is impermissible to use the inventor's disclosure as a "road map" for selecting and combining prior art disclosures. In Interconnect Planning Corp. v. Feil 774 F.2d 1132, 1143, 227 USPQ 542, 551 (Fed. Cir. 1985), the Federal Circuit noted that “The invention must be viewed not with the blueprint drawn by the inventor, but in the state of the art that existed at the time.”

The claimed features and limitations defined by claim 11 are not shown nor suggested in total combination of the references of record. Claim 11 is further patentable over the references of record.

The rejection of the claim 11 under 35 USC §103 is incorrect and should be reversed.

Claim 13 is patentable

Independent claim 13 recites apparatus for implementing deterministic based broken scan chain diagnostics in a computer test system connected to a Physical Failure Analysis system. Independent claim 13 recites a set of deterministic test patterns; each of the deterministic test pattern being a predetermined Level Sensitive Scan Design (LSSD) pattern. Independent claim 13 recites a test control program utilizing all potential system functional paths and all system clocks on a device under test, loading a deterministic test pattern into each scan chain in the device under test in a system mode using lateral insertion of respective deterministic values of the deterministic test pattern into each of a plurality of latches of each said scan chain via system data ports and applying system clocks to capture the respective deterministic values in each of the plurality of latches of each said scan chain.

Applicants respectfully submit that the recited limitations considered with the subject matter of independent claim 13 is not rendered obvious by the total teachings of the references of record including Sarrica and Rajski. No teaching, suggestion, or motivation provided by Sarrica and Rajski nor any general knowledge in

the art exists to achieve the subject matter of the invention, as claimed by Applicants in independent claim 13.

Independent claim 13 further recites that the test control program unloading each scan chain and identifying a last switching latch in each scan chain; repeating the generating, loading, unloading and identifying a last switching latch in each said scan chain testing steps a selected number of times with the deterministic test pattern; and checking for consistent results of the identified last switching latch in each scan chain and responsive to consistent results being identified, sending the identified last switching latch in each scan chain to said Physical Failure Analysis system to localize a physical defect; and responsive to consistent results not being identified, selecting another deterministic test pattern.

Applicants submit that the subject matter of the claimed invention as recited in claim 13 would not have been obvious to one of ordinary skill in the art in view of the references of record. No hint is found in the references of record and the references of record do not suggest the test control program unloading each scan chain and identifying a last switching latch in each scan chain, as taught and claimed by Applicants in claim 13.

There is no teaching or suggestion in any of the cited references, individually or taken as a whole, to make the claimed invention obvious. Thus, claim 13 is patentable.

Claim 19 is patentable

Independent claim 19 recites a computer program product for implementing deterministic based broken scan chain diagnostics of a device under test in a computer test system connected to a Physical Failure Analysis system, said computer program product including instructions stored on a computer recording medium consisting one of a floppy disk, an optically read compact disk, a compact disk read only memory (CD-ROM), and a tape, wherein said instructions, when executed by the computer test system to cause the computer system to perform the steps of.

Independent claim 19 recites that the deterministic test pattern being a predetermined Level Sensitive Scan Design (LSSD) pattern and the steps of utilizing all potential system functional paths and all system clocks on a device under test, loading the deterministic test pattern into each scan chain in the device under test in a system mode using lateral insertion of respective deterministic values of the deterministic test pattern into each of a plurality of latches of each said scan chain via system data ports and applying system clocks to capture the respective deterministic values in each of the plurality of latches of each said scan chain.

The above limitation and steps as recited in independent claim 19 are not disclosed or suggested by the combined teachings of the references of record including Sarrica et al. and Rajski. The system clocks are different from and are not equivalent to scan clocks for LSSD testing as taught by Sarrica et al. and Rajski.

Rejections based on § 103 must rest on a factual basis with these facts being interpreted without hindsight reconstruction of the invention from the prior art. The Examiner may not, because of doubt that the invention is patentable, resort to

speculation, unfounded assumption or hindsight reconstruction to supply deficiencies in the factual basis for the rejection. See In re Warner, 379 F.2d 1011, 1017, 154 USPQ 173, 178 (CCPA 1967), cert. denied, 389 U.S. 1057 (1968).

Independent claim 19 recites the steps of repeating the generating, loading, unloading and identifying a last switching latch in each said scan chain testing steps a selected number of times with the deterministic test pattern.

These steps as recited in independent claim 19 are not disclosed or suggested by the combined teachings of the references of record including Sarrica et al. and Rajski.

The computer program product as recited in independent claim 19 is patentable over the prior art.

E. CONCLUSION

Claims 1-2, 4-13, and 15-20 are patentable over all the references of record and are not rendered obvious by the prior art. Each of the claims 1-2, 4-13, and 15-20 is patentable and the Examiner's rejections should be reversed.

It is respectfully requested that the final rejection be reversed.

Respectfully submitted,

S-signature by

___/Joan Pennington/_____
By: Joan Pennington
Reg. No. 30,885
Telephone: (312) 670-0736

December 26, 2007

(8) CLAIMS APPENDIX

CLAIMS ON APPEAL

1. A method for implementing deterministic based broken scan chain diagnostics using a computer test system connected to a Physical Failure Analysis system comprising the steps of:

generating a deterministic test pattern using a base deterministic test pattern set generated by an Automatic Test Pattern Generation (ATPG) system; the deterministic test pattern being a predetermined Level Sensitive Scan Design (LSSD) pattern;

utilizing all potential system functional paths and all system clocks on a device under test, loading the deterministic test pattern into each scan chain in the device under test in a system mode using lateral insertion of respective deterministic values of the deterministic test pattern into each of a plurality of latches of each said scan chain via system data ports and applying system clocks to capture the respective deterministic values in each of the plurality of latches of each said scan chain;

unloading each scan chain and identifying a last switching latch in each said scan chain;

repeating the generating, loading, unloading and identifying a last switching latch in each said scan chain testing steps a selected number of times with the deterministic test pattern;

checking for consistent results of the identified last switching latch in each scan chain; and responsive to consistent results being identified, sending the identified last switching latch in each scan chain to said Physical Failure Analysis system to localize a

physical defect; and

responsive to consistent results not being identified, selecting another deterministic test pattern.

2. A method for implementing deterministic based broken scan chain diagnostics as recited in claim 1 further includes the steps of repeating the testing steps a selected number of times with the selected deterministic test pattern.

3. (canceled)

4. A method for implementing deterministic based broken scan chain diagnostics as recited in claim 1 wherein the step of generating a deterministic test pattern includes the steps of using perturbations of one base deterministic test pattern from said base deterministic test pattern set generated by said Automatic Test Pattern Generation (ATPG) system.

5. A method for implementing deterministic based broken scan chain diagnostics as recited in claim 4 wherein the step of using perturbations of one base deterministic test pattern includes the steps of applying said one base deterministic test pattern from the base deterministic test pattern set to an exclusive OR and multiplexing a selected perturbation matrix entry using said exclusive OR.

6. A method for implementing deterministic based broken scan chain diagnostics as recited in claim 5 includes the steps of providing a perturbation matrix with a plurality of perturbation matrix entries including selected ones of no invert, all invert, a predefined bit invert; rotate, and invert rotate.

7. A method for implementing deterministic based broken scan chain diagnostics as recited in claim 1 wherein the step of generating a deterministic test pattern includes the steps of using a software Pseudo Random Pattern Generator (PRPG).

8. A method for implementing deterministic based broken scan chain diagnostics as recited in claim 1 wherein the step of generating a deterministic test pattern includes the steps of using a set of deterministic test patterns resident in a memory.

9. A method for implementing deterministic based broken scan chain diagnostics as recited in claim 1 wherein the step of loading the deterministic test pattern into each scan chain in the device under test using lateral insertion via system data ports and applying system clocks includes the steps of applying deterministic values of the deterministic test pattern to a selected one of scan chain inputs and primary inputs of latches within each scan chain.

10. A method for implementing deterministic based broken scan chain diagnostics as recited in claim 1 wherein the step of loading the deterministic test pattern into each scan chain in the device under test using lateral insertion via system data ports and applying system clocks includes the steps of applying perturbation deterministic values of the deterministic test pattern to a selected one of scan chain inputs and primary inputs of latches within each scan chain.

11. A method for implementing deterministic based broken scan chain diagnostics as recited in claim 1 wherein the step of loading the deterministic test

pattern into each scan chain in the device under test using lateral insertion via system data ports and applying system clocks includes the steps of applying random data from a software Pseudo Random Pattern Generator (PRPG) to scan chain inputs and primary inputs of latches within each scan chain.

12. A method for implementing deterministic based broken scan chain diagnostics as recited in claim 1 wherein the step of loading the deterministic test pattern into each scan chain in the device under test using lateral insertion via system data ports and applying system clocks includes the steps of applying output values from an exclusive OR receiving one base deterministic test pattern from a base deterministic test pattern set and a selected perturbation matrix entry.

13. Apparatus for implementing deterministic based broken scan chain diagnostics in a computer test system connected to a Physical Failure Analysis system comprising:

a set of deterministic test patterns; said set of deterministic test patterns being generated using a base deterministic test pattern set generated by an Automatic Test Pattern Generation (ATPG) system in a computer test system; each of the deterministic test pattern being a predetermined Level Sensitive Scan Design (LSSD) pattern;

a test control program utilizing all potential system functional paths and all system clocks on a device under test, loading a deterministic test pattern into each scan chain in the device under test in a system mode using lateral insertion of respective deterministic values of the deterministic test pattern into each of a plurality of latches of each said scan chain via system data ports and applying system clocks to capture the

respective deterministic values in each of the plurality of latches of each said scan chain; unloading each scan chain and identifying a last switching latch in each scan chain; repeating the generating, loading, unloading and identifying a last switching latch in each said scan chain testing steps a selected number of times with the deterministic test pattern; and checking for consistent results of the identified last switching latch in each scan chain and responsive to consistent results being identified, sending the identified last switching latch in each scan chain to said Physical Failure Analysis system to localize a physical defect; and responsive to consistent results not being identified, selecting another deterministic test pattern.

14. (canceled)

15. Apparatus for implementing deterministic based broken scan chain diagnostics as recited in claim 13 wherein said set of deterministic test patterns includes perturbations of one base deterministic test pattern from said base deterministic test pattern set generated by said Automatic Test Pattern Generation (ATPG) system.

16, Apparatus for implementing deterministic based broken scan chain diagnostics as recited in claim 15 wherein said perturbations of one base deterministic test pattern is generated by applying said one base deterministic test pattern from the base deterministic test pattern set to an exclusive OR and multiplexing a selected perturbation matrix entry using said exclusive OR.

17. Apparatus for implementing deterministic based broken scan chain diagnostics as recited in claim 16 includes a perturbation matrix having a plurality of

perturbation matrix entries including selected ones of no invert, all invert, a predefined bit invert; rotate, and invert rotate.

18. Apparatus for implementing deterministic based broken scan chain diagnostics as recited in claim 13 wherein said set of deterministic test patterns includes a software Pseudo Random Pattern Generator (PRPG) for generating a deterministic test pattern.

19. A computer program product for implementing deterministic based broken scan chain diagnostics of a device under test in a computer test system connected to a Physical Failure Analysis system, said computer program product including instructions stored on a computer recording medium consisting one of a floppy disk, an optically read compact disk, a compact disk read only memory (CD-ROM), and a tape, wherein said instructions, when executed by the computer test system to cause the computer system to perform the steps of:

generating a deterministic test pattern using a base deterministic test pattern set generated by an Automatic Test Pattern Generation (ATPG) system; the deterministic test pattern being a predetermined Level Sensitive Scan Design (LSSD) pattern;

utilizing all potential system functional paths and all system clocks on a device under test, loading the deterministic test pattern into each scan chain in the device under test in a system mode using lateral insertion of respective deterministic values of the deterministic test pattern into each of a plurality of latches of each said scan chain via system data ports and applying system clocks to capture the respective deterministic values in each of the plurality of latches of each said scan chain;

unloading each scan chain and identifying a last switching latch in each scan chain;

repeating the generating, loading, unloading and identifying a last switching latch in each said scan chain testing steps a selected number of times with the deterministic test pattern;

checking for consistent results of the identified last switching latch in each scan chain; and responsive to consistent results being identified with the deterministic test pattern, sending the identified last switching latch in each scan chain to said Physical Failure Analysis system to localize a physical defect; and

responsive to consistent results not being identified, selecting another deterministic test pattern.

20. A computer program product for implementing deterministic based broken scan chain diagnostics as recited in claim 19 includes the steps responsive to consistent results not being identified, repeating the generating, loading, unloading and identifying a last switching latch in each said scan chain testing steps a selected number of times with the selected deterministic test pattern.

(9) EVIDENCE APPENDIX

None.

(10) RELATED PROCEEDINGS APPENDIX

None.